PATENT APPLICATION
DOCKET NO.: 200315314-1

REMARKS

Claims 1-5, 7-13, 15-20 and 22 are presented for examination, of which claims 1, 9 and 16 are in independent form.

Claims 1, 7, 9, 15, 16 and 22 have been amended by way of the present response. Additionally, claims 6, 14 and 21 have been cancelled without estoppel, prejudice, limitation or waiver. No new matter is introduced hereby.

Support for the claim amendments of the present response may be found, *inter alia*, in FIGS. 1B and 2, for example, as well as the related description at Paragraphs [0012]-[0013] and [0023]-[0024] of the specification of the instant application.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Claim Rejections - 35 U.S.C. §102(b)

Claims 1-22 are rejected in the pending Office Action under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,300,100 to Marchelli (hereinafter the *Marchelli* reference). In connection with these rejections, the Examiner has commented as follows with respect to base claim 1:

> Marchelli's Fig. 4 shows a system for detecting an edge of a data signal (c) carried on an observability bus, the system comprising:
>
> a first performance counter (FF') connected to receive said data signal, said first performance counter being operable to assert a trigger signal (d) in a given clock cycle in response to detecting an assertion of said data signal in the previous clock cycle (clearly shown in Fig. 4a); and
>
> a second performance counter (G and FF") connected to receive said data signal and said trigger signal, wherein said second performance counter detects said edge based on said assertion of said data signal (when signals c and b are asserted so is the output f) and a logic level in said trigger signal that is a complement to a logic level associated with said assertion of said data signal.

Substantially identical reasons are also provided in the pending Office Action with respect the rejection of base claims 9 and 16.

Applicant respectfully submits that the foregoing §102(b) rejections have been overcome or otherwise rendered moot by way of the present amendment and offers the following discussion as support. As defined by the base claim 1, an embodiment of the present disclosure is directed to a system for counting occurrences of an edge of a data signal carried on an observability bus. As currently constituted, the claimed system

comprises, *inter alia*, a first performance counter connected to receive the data signal, the first performance counter connected to assert a trigger signal in a given clock cycle in response to detecting an assertion of the data signal in the previous clock cycle. The system further comprises a second performance counter connected to receive the data signal and the trigger signal, wherein the second performance counter counts an occurrence of the edge when the data signal is asserted and the trigger signal has a logic level that is a complement to a logic level associated with the assertion of the data signal.

Base claims 9 and 16 contain similar features. Claim 9 is directed to an embodiment of a method for counting occurrences of an edge of a data signal carried on an observability bus. Claim 16 is directed to a second embodiment of a system for counting occurrences of an edge of a data signal carried on an observability bus.

As noted previously, the *Marchelli* reference is directed to providing a circuit arrangement for correlating the operation of two or more multistage counters (each counter possibly including a primary and secondary chain of binary stages) which are driven

substantially at the same frequency but having indeterminate phase relationships. See column 1, lines 45-50. Cited FIG. 4 of *Marchelli* and accompanying FIG. 4A, both of which are reproduced herein for convenience, illustrate a correlation circuit and exemplary signals associated with the circuit.

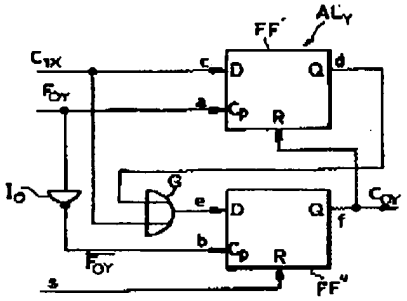

FIG.4

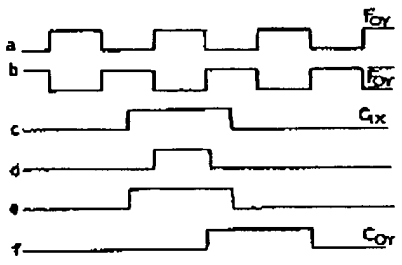

FIG 4a

The circuit of FIG. 4 contains two flip-flop circuits FF' and FF". Flip-flop FF' receives a restarting signal C_{1X} as data and a clock signal F_{OY} as switching input to generate a high pulse on output signal **d** when restart signal C_{1X} is high on a rising edge of clock signal F_{OY}. Flip-flop FF" receives the inverse of clock signal F_{OY} (i.e., $/F_{OY}$) as its switching input. Further, flip-flop FF" also receives, as data, signal **e**, which is the output of OR gate **G** (note that while gate **G** appears to be pictured as an

AND gate, *Marchelli* describes gate **G** as an OR gate and the value of output **e** relative to the value of inputs C_{1X} and **d** corresponds to that of an OR gate). Flip-flop FF" outputs a high signal on C_{OY} when either of signals C_{1X} or **d** is high on the rising edge of clock signal $/F_{OY}$. *Marchelli* notes that flip-flop FF' is needed only to ensure that command C_{OY} is still generated by the circuit if the arrival of pulse C_{1X} coincides so closely with a leading edge of a pulse on $/F_{OY}$ that flip-flop FF" could fail to switch on either this or the next-following inverted clock pulse. See column 5, lines 9-54.

Flip-flop FF" does not count an occurrence of an edge when "data signal" C_{1X} is asserted and "trigger signal" **d** has a logic level that is a complement to a logic level associated with the assertion of C_{1X}, as is now recited in claim 1.

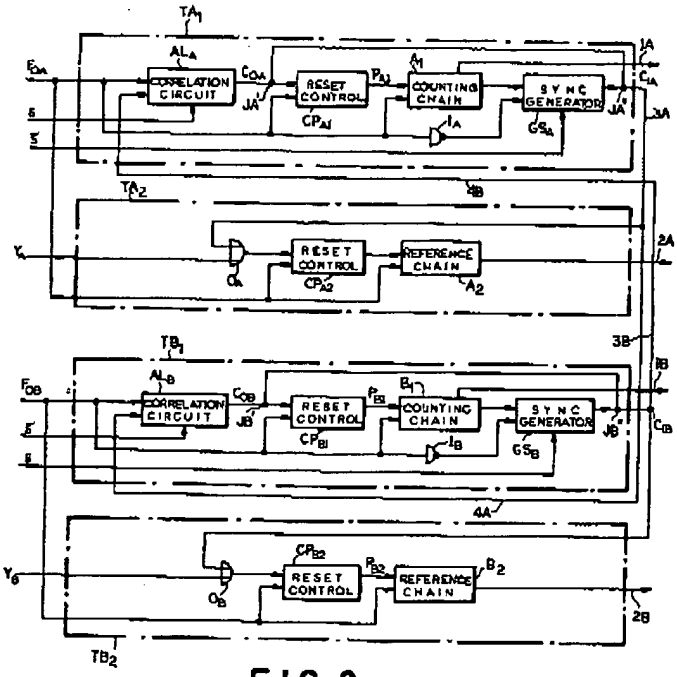

FIG. 2

Further, the circuit shown in FIG. 4 does not perform counting; rather, the output of the circuit, C_{OX}, serves as a command signal to other elements in a larger circuit.

While *Marchelli* does disclose a counting chain in FIG. 2, also reproduced herein for convenience, counting chains A_1 and B_1 count clock cycles of signals F_{OA}, F_{OB} in order to trigger SYNC generators GS_A, GS_B to generate sync signals. See column 3, lines 32-46. Accordingly, *Marchelli* does not meet the limitation relating to a second performance counter counting an occurrence of the edge when the data signal is asserted and the trigger signal has a logic level that is a complement to a logic level associated with the assertion of the data signal, as recited in claim 1.

Based on the foregoing, Applicant respectfully submits that base claim 1 is not anticipated or suggested by the *Marchelli* reference, and is therefore believed to be in condition for allowance. Base claims 9 and 16 contain the same distinguishing features and are also believed to be in condition for allowance. Claims 2-5, 7 and 8 depend from the base claim 1 and introduce additional limitations therein. Likewise, claims 10-13 and 15

depend from base claim 9 and claims 17-20 and 22 depend from base claim 16, each introducing additional limitations therein. Accordingly, these dependent claims are also believed to be in condition for allowance.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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